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Drake et al.

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(54) **COMPUTER SYSTEM FOR ALLOWING A TWO WORD JUMP INSTRUCTION TO BE EXECUTED IN THE SAME NUMBER OF CYCLES AS A SINGLE WORD JUMP INSTRUCTION**

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(58) **Field of Search** 711/211, 214, 711/220; 712/24, 205, 206, 215

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(57) **ABSTRACT**

A system for allowing a two word jump instruction to be executed in the same number of cycles as a single word jump instruction, thereby allowing a processor system to increase memory space without reducing performance. A first address bus is coupled to the linearized program memory for sending addresses of instructions to be fetched to a linearized program memory. A pointer is coupled to the first address bus for storing an address location of a current instruction in the linearized program memory to be fetched and for placing the address location of the current instruction to be fetched on the first address bus. A second address bus is provided and has one end coupled to the output of the program memory and a second end coupled to the first address bus. The second address bus is used for placing an address of an operand of a second word of the two word jump instruction onto the first address bus after an address of an operand of a first word of the two word jump instruction has been placed on the first address bus. This allows the addresses of the first word and the second word to be combined to provide the full address value of the two word jump instruction in the same number of cycles as a single word jump instruction.

13 Claims, 1 Drawing Sheet

