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(54) **LAYOUT TECHNIQUE FOR A MATCHING CAPACITOR ARRAY USING A CONTINUOUS TOP ELECTRODE**

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(58) **Field of Search** 257/532, 535, 257/750

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(57) **ABSTRACT**

A matching capacitor array is implemented on a single, monolithic integrated circuit. The array features a matrix of bottom electrodes and a plurality of continuous top electrode strips, where each continuous top electrode strip spans numerous bottom electrodes. The conductive contacts for each continuous top electrode strip are removed from the capacitor interface to the terminal ends of each of the continuous top electrode strips. The invention seeks to match or control parasitic and fringe capacitance, rather than to eliminate or minimize such capacitances. By creating a matched array, the parasitic and fringe capacitances of each matching capacitor unit cell are incorporated into the total capacitance of the unit cell.

6 Claims, 7 Drawing Sheets

