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Yach

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[54] **VOLTAGE REGULATOR AND BOOSTING CIRCUIT FOR READING A MEMORY CELL AT LOW VOLTAGE LEVELS**

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[52] **U.S. Cl.** **365/189.66**; 365/203; 365/185.18; 365/194

[58] **Field of Search** 365/189.06, 185.18, 365/189.11, 203, 194

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,801,991	9/1998	Keeney et al.	365/185.18
5,815,445	9/1998	Hull et al.	365/189.06

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[57] **ABSTRACT**

A system for reading a memory cell of a memory array at voltage levels lower than an erased threshold voltage of the memory array. The system uses a voltage regulator which is coupled to the memory array for charging a desired row of the memory array to a supply voltage. The voltage regulator is further used for clamping the desired row at a voltage level which is no higher than a maximum programmed threshold voltage of the memory array. The voltage regulator is able to perform these functions while consuming no DC current. A voltage booster is coupled to the voltage regulator and to the memory array. The voltage booster is used for raising the voltage level of the desired row to a voltage above the maximum erased threshold voltage of the memory cell. This allows the memory cell to be read at voltage levels which are lower than the threshold voltage of the memory array.

25 Claims, 1 Drawing Sheet

