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[54] **DIELECTRIC LAYER OF A MEMORY CELL HAVING A STACKED OXIDE SIDEWALL AND METHOD OF FABRICATING SAME**

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[52] **U.S. Cl.** **438/261**; 438/265; 438/258

[58] **Field of Search** 438/261, 265, 438/258

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,063,172	11/1991	Manley .	
5,104,819	4/1992	Freiberger et al. .	
5,158,092	10/1992	Hanada .	
5,420,060	5/1995	Gill et al. .	
5,790,455	8/1998	Caywood	365/185.06
5,836,772	11/1998	Chang et al.	438/265
5,856,221	1/1999	Clementi et al.	438/258
5,985,719	11/1999	Keller et al.	438/265

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[57] **ABSTRACT**

A merged two-transistor memory cell of an EEPROM, and method of fabricating the cell, are provided. The memory cell includes a substrate and gate oxide layer formed on the substrate. It also includes a memory transistor having a floating gate and a control gate, and a select transistor having a gate that is shared with the memory transistor. The memory cell is configured so that the shared gate serves both as the control gate of the memory transistor and the wordline of the select transistor. The memory cell further includes a dielectric layer that is disposed between the floating gate and the shared gate. The dielectric layer is defined by an ONO film and a stacked oxide layer. In fabricating the memory cell, the ONO stack film is formed adjacent to the top surface of the floating gate and the stacked oxide layer is formed adjacent to the side surface of the floating gate.

11 Claims, 7 Drawing Sheets

