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[54] **DATA POINTER FOR OUTPUTTING INDIRECT ADDRESSING MODE ADDRESSES WITHIN A SINGLE CYCLE AND METHOD THEREFOR**

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[52] **U.S. Cl.** **711/200**; 712/43; 711/219; 711/220

[58] **Field of Search** 711/211, 214, 711/219, 220, 200, 212; 712/220, 43

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[57] **ABSTRACT**

A data pointer for generating an indirect addressing mode address within a single cycle for a selected one of a plurality of multiple indirect addressing modes. The data pointer is used with a processor architecture scheme which allows for encoding of multiple addressing modes. A data pointer register is coupled to the processor architecture scheme for storing a current address of an operand to be used in a simple indirect addressing mode. An incrementer is coupled to the data pointer register for incrementing the current address of an operand to be used in a simple indirect data addressing mode by a set number thereby generating an address of an operand to be used in an indirect addressing mode with auto preincrement. An adder is coupled to the data pointer register for combining the current address of an operand to be used in a simple indirect data addressing mode with an offset number thereby generating an address of an operand to be used in an indirect addressing mode with offset. A multiplexer circuit is coupled to an output of the data pointer register, to an output of the incrementer, and to an output of the adder for selecting a desired indirect addressing mode address.

12 Claims, 2 Drawing Sheets

