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[54] **PROCESSOR ARCHITECTURE SCHEME HAVING MULTIPLE BANK ADDRESS OVERRIDE SOURCES FOR SUPPLYING ADDRESS VALUES AND METHOD THEREFOR**

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[58] **Field of Search** 395/800.38, 800.32, 395/800.01, 800.39, 800.34; 712/38, 32, 1, 39, 34

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,047,245	9/1977	Knipper	711/213
4,118,773	10/1978	Joyce et al. .	
4,685,084	8/1987	Canepa .	
5,247,644	9/1993	Johnson et al.	711/157
5,751,988	5/1998	Fujimura	395/405

FOREIGN PATENT DOCUMENTS

0 463 855 A2 1/1992 European Pat. Off. .

0 518 479 A2 12/1992 European Pat. Off. .

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[57] **ABSTRACT**

A processor architecture scheme which allows for encoding multiple addressing modes and which has multiple sources for generating a bank address value. The processor architecture scheme has a Central Processing Unit (CPU) for executing an instruction set. A data memory is coupled to the CPU. The data memory is used for storing and transferring data to and from the CPU. The data memory is divided into a plurality of banks wherein one of the plurality of banks is a dedicated bank for general and special purpose registers. A selection circuit is coupled to the data memory. The selection circuit is used for selecting one of the multiple sources for generating the bank address value. A bank select register is coupled to the selection circuit. The bank select register is used for supplying a bank address value for an instruction to be executed in a direct short addressing mode. An instruction register is coupled to the selection circuit for supplying a bank address values for an instruction to be executed in a direct long addressing mode and for supplying a register address within a bank for the instruction to be executed in a direct short addressing mode.

5 Claims, 2 Drawing Sheets

