US005987583A

United States Patent [19]

Triece et al.

[11] Patent Number: 5,987,583

[45] Date of Patent: Nov. 16, 1999

[54] **PROCESSOR ARCHITECTURE SCHEME AND INSTRUCTION SET FOR MAXIMIZING AVAILABLE OPCODES AND ADDRESS SELECTION MODES**

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[21] Appl. No.: **08/959,942**

[22] Filed: **Oct. 29, 1997**

Related U.S. Application Data

[63] Continuation-in-part of application No. 08/946,426, Oct. 7, 1997.

[51] **Int. Cl.**[6] **G06F 9/34**

[52] **U.S. Cl.** **711/214**; 711/219; 712/220

[58] **Field of Search** 711/214, 220, 711/219; 395/376; 712/220

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[57] **ABSTRACT**

A system for allowing multiple addressing modes while maximizing a number of available opcodes and addressable registers. The system has a processor architecture scheme which allows for encoding of multiple addressing modes through use of virtual register addresses. The system has an instruction set having a plurality of instructions. Each instruction has a plurality of bits wherein none of the plurality of bits in each of the plurality of instructions are dedicated bits for implementing different addressing modes. Each of the plurality of instructions are able to implement different addressing modes by addressing the virtual register addresses in the processor architecture scheme. Since no bits are required for implementing different addressing modes, the length of the opcode field and the register address field are determined by the number of opcodes and the number of addressable registers the user wishes to implement.

10 Claims, 2 Drawing Sheets

