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Chiao et al.

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[54] **PHASE LOCKED LOOP WITH IMPROVED LOCK TIME AND STABILITY**

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[58] **Field of Search** ..... 375/376; 331/25, 331/18, 17, 1 A, 1 R; 327/157, 156; 455/260

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[57] **ABSTRACT**

A phase-locked loop (PLL) circuit is used to synchronize a local clock frequency with an edge of a reference clock frequency, employing a phase detector to compare the local clock frequency and the reference clock frequency to generate a control signal indicative of the need to increase or to decrease the local clock frequency for phase locking thereof to the reference clock frequency. A voltage controlled oscillator (VCO) is responsive to a signal voltage derived from the control signal to vary the local clock frequency as necessary to achieve phase locking. A loop filter has a reference voltage threshold level which is pre-programmable to enable the loop filter to respond to the control signal by adjusting the signal voltage as a virtual step function toward the programmed reference voltage threshold level before application to the VCO, and then cycling up and down in a search for a stable control signal voltage to reduce the time necessary to achieve the desired phase locking.

8 Claims, 3 Drawing Sheets

