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Wojewoda et al.

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[54] **PHASE LOCKED LOOP WITH FAST START-UP CIRCUITRY**

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[58] **Field of Search** ..... 331/1 A, 4, 8, 331/16, 17, 25, DIG. 2; 327/105–107, 156–159

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[57] **ABSTRACT**

A phase-locked loop (PLL) circuit has a phase comparator for comparing the phases of a local clock frequency and a reference frequency to generate a control signal indicative of a direction of adjustment of the local clock frequency for reducing the phase difference between the two frequencies. A voltage controlled oscillator (VCO) of the PLL responds to application of a control voltage thereto to generate an oscillation signal frequency from which the local clock frequency is derived. A loop filter responds to the control signal from the phase comparator to develop a control voltage for application to the VCO to adjust the local clock frequency in the direction indicated by the control signal to reduce the relative phase difference. The loop filter has a start-up circuit for detecting a selected edge of a cycle of the reference frequency after a predetermined number of cycles following commencement of operation or reset of the PLL circuit as being indicative of stabilization of the reference frequency, and is responsive to detection of such selected edge for promptly producing a linear boost of the control voltage from an initial level of substantially zero volts to a predetermined pull-up level exceeding the level of control voltage required to achieve phase locking. This reduces the time interval required to achieve phase locking, measured from the selected cycle edge. The loop filter is also responsive to the control voltage reaching the pull-up level to incrementally reduce the control voltage to the level required to achieve phase locking.

19 Claims, 3 Drawing Sheets

