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[54] **VOLTAGE REFERENCE GENERATOR FOR EPROM MEMORY ARRAY**

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[52] **U.S. Cl.** **365/189.09**; 365/189.06; 365/185.2

[58] **Field of Search** 365/189.09, 189.06, 365/189.11, 185.23, 185.2, 226; 395/750

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[57] **ABSTRACT**

A technique is disclosed for reading a memory element of an EPROM array embedded in a microcontroller chip which has been scaled down from a previous design by virtue of reduced line widths of a process technology used for fabricating the chip. The microcontroller chip has a predetermined supply voltage, and the array comprises rows and columns of addressable memory elements which may be selectively accessed to read data content therefrom in a low voltage mode in which the supply voltage initially rises and ultimately reaches substantially its maximum voltage during a read cycle. A regulated reference voltage is used to exercise row and column control in the low voltage read mode by tracking the level of the supply voltage up to a certain preselected level below the maximum supply voltage, and by clamping the row and column control voltage at substantially the preselected level despite increases in the level of the supply voltage above the preselected level.

9 Claims, 2 Drawing Sheets

