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[54] **OVERCHARGE/DISCHARGE VOLTAGE REGULATOR FOR EPROM MEMORY ARRAY**

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[52] **U.S. Cl.** ..... **365/185.25**; 365/20 W

[58] **Field of Search** 365/185.25, 204, 365/185.04, 185.18, 185.21, 189.01

[56] **References Cited**

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[57] **ABSTRACT**

A method of high speed reading of data from an EPROM, in which a memory array is programmed based on device status at intersections of rows and columns of the array to store data therein as 0's and 1's, uses a capacitive overcharging and discharging technique to enable fast voltage stabilization without drawing significant current. A row containing the memory element to be read is quickly overdriven to overcharge an effective capacitance associated with the row to substantially the maximum level of the EPROM supply voltage which may exceed the programmed threshold voltage of the selected memory element. The effective capacitance is thereupon discharged to a predetermined voltage level below both the maximum level of the supply voltage and the programmed threshold. Then the status and data content of the selected memory element are read by first grounding an electrode of a source-drain path of a transistor comprising the memory element to cause current with substantially no DC component to flow through that path of the transistor. A sense amplifier in the source-drain path of the transistor is triggered to detect current flow therethrough as indicative of the data content of the memory element.

9 Claims, 2 Drawing Sheets

