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[54] **SERIAL EEPROM DEVICE AND ASSOCIATED METHOD FOR REDUCING DATA LOAD TIME USING A PAGE MODE WRITE CACHE**

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[51] **Int. Cl.**[6] **G06F 13/28**; G06F 13/36; G11C 16/04

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[58] **Field of Search** 395/425, 430, 395/445, 453; 365/185, 900, 230.03, 238.5

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[57] **ABSTRACT**

A serial EEPROM (electrically erasable programmable read only memory) device and method for reducing the time required to load data into the serial EEPROM device using a special write cache are disclosed. The EEPROM has an internal memory array for receiving a burst of data sent by a microcontroller. Data in the burst of data is initially loaded into an SRAM (static random access memory) write cache where it is stored sequentially and grouped in a plurality of pages, so that the bus and the microcontroller are freed to allow the microcontroller to perform other processing tasks at least until the EEPROM memory is written and the EEPROM is again accessible to the microcontroller. Writing of the internal memory array is accomplished sequentially with data from the pages of the cache loaded into rows of the internal memory array until the cache is depleted, the pages being sized so that an integral number of pages is stored in each row of the internal memory array.

5 Claims, 3 Drawing Sheets

