US005473758A

United States Patent [19]

Allen et al.

[11] Patent Number: 5,473,758

[45] Date of Patent: Dec. 5, 1995

[54] **SYSTEM HAVING INPUT OUTPUT PINS SHIFTING BETWEEN PROGRAMMING MODE AND NORMAL MODE TO PROGRAM MEMORY WITHOUT DEDICATING INPUT OUTPUT PINS FOR PROGRAMMING MODE**

[75] Inventors: **Ray Allen**, Mesa; **Sumit Mitra**, Tempe; **Rodney Drake**, Mesa, all of Ariz.

[73] Assignee: **Microchip Technology Incorporated**, Chandler, Ariz.

[21] Appl. No.: **938,911**

[22] Filed: **Aug. 31, 1992**

[51] **Int. Cl.**[6] **G06F 15/02**

[52] **U.S. Cl.** **395/430**; 395/834; 364/232.9; 364/244.6; 364/716; 364/DIG. 1; 365/52

[58] **Field of Search** 395/275, 375, 395/500, 425, 800; 364/232.8, 232.9, 221.6, 244.6, 946.2, 946.9, 949.2, 965.76, 716; 307/465, 449, 450, 468; 365/52

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,680,731	7/1987	Izumi et al.	364/200
4,785,425	11/1988	Lavelle	365/52
4,896,296	1/1990	Turner et al.	307/465
5,222,046	6/1993	Kreifels et al.	365/230.06
5,237,218	8/1993	Josephson et al.	307/465
5,276,839	1/1994	Robb et al.	395/425
5,336,951	8/1994	Josephson et al.	307/465

Primary Examiner—Thomas C. Lee
Assistant Examiner—Moustafa M. Meky
Attorney, Agent, or Firm—O'Connor Cavanagh

[57] **ABSTRACT**

A microcontroller and associated EPROM program memory are fabricated in a single semiconductor chip. The microcontroller device is adapted to be programmed using digital command words or other bit patterns applied as inputs after installation of the device in circuit with a system to be controlled by the device, and to have its programming pins isolated from the system to avoid effects on system operation while the programming is taking place. The in-circuit programming uses considerably less than the total number of input/output (I/O) pins of the device, which in total are fewer than the number of bits in a command word. This is achieved with a serial/parallel programming interface between the pins and the program memory, and by applying the data in serial fashion to the interface where it is latched and loaded in parallel in the memory. Input data to the device may alternatively be entered in parallel to the interface in bytes of width less than the total number of I/O pins of the device.

10 Claims, 1 Drawing Sheet

