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[54] **SYSTEM FOR SINGLE CYCLE TRANSFER OF UNMODIFIED DATA TO A NEXT SEQUENTIALLY HIGHER ADDRESS IN A SEMICONDUCTOR MEMORY**

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[52] **U.S. Cl.** **395/425**; 365/189.04; 364/DIG. 1; 364/244.3; 364/251.1; 364/260

[58] **Field of Search** 364/200, 900; 365/230.08, 230.06, 189.04, 230.04, 230.09; 395/800, 425

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[57] **ABSTRACT**

The RAM includes sub-arrays having odd and even memory locations, respectively. A data move instruction results in externally generated row and column address signals which are decoded to cause a first memory location, in one of the sub-arrays, to be selected and data to be read. The next memory location in sequence, in the other of the sub-arrays, is then selected, without necessity for an additional set of row address signals, for writing of the read information. The row decoder includes row indexing circuitry actuatable upon receipt of a shift signal signifying that the first memory location is in the last column of a given row. When the shift signal is received, the write location is automatically selected to be in the succeeding row.

4 Claims, 4 Drawing Sheets

