US012346722B2

(12) **United States Patent**
Catherwood et al.

(10) **Patent No.: US 12,346,722 B2**
(45) **Date of Patent: Jul. 1, 2025**

(54) **SYSTEMS AND METHODS FOR MANAGING INTERRUPT PRIORITY LEVELS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 489 days.

(21) Appl. No.: **18/073,075**

(22) Filed: **Dec. 1, 2022**

(65) **Prior Publication Data**

US 2023/0176898 A1 Jun. 8, 2023

Related U.S. Application Data

(60) Provisional application No. 63/286,634, filed on Dec. 7, 2021.

(51) **Int. Cl.**
G06F 9/48 (2006.01)
G06F 8/71 (2018.01)

(52) **U.S. Cl.**
CPC ***G06F 9/4831*** (2013.01); ***G06F 8/71*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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(57) **ABSTRACT**

A system includes non-transitory computer readable memory and a processor. The non-transitory computer readable memory stores a current processor interrupt priority level and a current disable interrupt control (DISICTL) interrupt priority level. The processor to update the current processor interrupt priority level based on respective interrupt priority levels associated with respective exceptions, and update the current DISICTL interrupt priority level based on a respective DISICTL instruction, wherein the respective DISICTL instruction specifies a respective user-definable DISICTL interrupt priority level. The processor determines a highest interrupt priority level between the current processor interrupt priority level and the current DISICTL interrupt priority level, and apply the highest interrupt priority level during execution of respective code.

20 Claims, 7 Drawing Sheets

