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(54) **SYSTEMS AND METHODS FOR MANAGING INTERRUPT PRIORITY LEVELS**

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CPC ***G06F 9/4831*** (2013.01); ***G06F 8/71*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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(57) **ABSTRACT**

A system includes non-transitory computer readable memory and a processor. The non-transitory computer readable memory stores a current processor interrupt priority level and a current disable interrupt control (DISICTL) interrupt priority level. The processor to update the current processor interrupt priority level based on respective interrupt priority levels associated with respective exceptions, and update the current DISICTL interrupt priority level based on a respective DISICTL instruction, wherein the respective DISICTL instruction specifies a respective user-definable DISICTL interrupt priority level. The processor determines a highest interrupt priority level between the current processor interrupt priority level and the current DISICTL interrupt priority level, and apply the highest interrupt priority level during execution of respective code.

20 Claims, 7 Drawing Sheets