US012314123B2

(12) **United States Patent**
Reiter et al.

(10) **Patent No.: US 12,314,123 B2**
(45) **Date of Patent: May 27, 2025**

(54) **PROGRAMMABLE FAULT VIOLATION FILTER**

(71) Applicant: **Microchip Technology Incorporated**, Chandler, AZ (US)

(72) Inventors: **Andreas Reiter**, Feldkirchen-Westerham (DE); **Yong Yuenyongsgool**, Gilbert, AZ (US); **Stephen Bowling**, Chandler, AZ (US); **Alex Dumais**, Boise, ID (US); **Justin Oshea**, Chandler, AZ (US); **Sankar Rangarajan**, Chandler, AZ (US)

(73) Assignee: **Microchip Technology Incorporated**, Chandler, AZ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 69 days.

(21) Appl. No.: **18/096,163**

(22) Filed: **Jan. 12, 2023**

(65) **Prior Publication Data**

US 2023/0393923 A1 Dec. 7, 2023

Related U.S. Application Data

(60) Provisional application No. 63/348,383, filed on Jun. 2, 2022.

(51) **Int. Cl.**
G06F 11/00 (2006.01)
G06F 11/07 (2006.01)

(52) **U.S. Cl.**
CPC ***G06F 11/0772*** (2013.01); ***G06F 11/076*** (2013.01); ***G06F 11/0781*** (2013.01)

(58) **Field of Classification Search**
CPC . G06F 11/0772; G06F 11/076; G06F 11/0781
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2011/0153236	A1	6/2011	Montreuil et al.	702/59
2014/0218316	A1 *	8/2014	Chen	G06F 11/3062 345/173
2015/0330841	A1	11/2015	Kern et al.	700/275
2016/0266605	A1 *	9/2016	Hegde	G06F 1/06
2023/0393923	A1 *	12/2023	Reiter	G06F 11/0781

OTHER PUBLICATIONS

International Search Report and Written Opinion, Application No. PCT/US2023/024295, 10 pages.

* cited by examiner

Primary Examiner — Philip Guyton
(74) *Attorney, Agent, or Firm* — SLAYDEN GRUBERT BEARD PLLC

(57) **ABSTRACT**

A fault event monitor and filter having a digital comparator receiving a digital input value, wherein the digital comparator generates a plurality of outputs based on programmable threshold input values, a first counter coupled to a first output of the plurality of outputs of the digital comparator, a second counter coupled to a second output of the plurality of outputs of the digital comparator, and an output controller with a first input coupled to an output of the first counter and with a second input coupled to an output of the second counter, wherein the output controller to generate a fault event signal based at least partially on signals received from the first and second counters.

9 Claims, 5 Drawing Sheets