

(12) **United States Patent**
Daryanani

(10) **Patent No.:** **US 12,313,476 B2**
(45) **Date of Patent:** **May 27, 2025**

(54) **TEMPERATURE SENSOR INTEGRATED IN A TRANSISTOR ARRAY**

USPC 257/470
See application file for complete search history.

(71) Applicant: **Microchip Technology Incorporated,**
Chandler, AZ (US)

(56) **References Cited**

(72) Inventor: **Sonu Daryanani,** Tempe, AZ (US)

U.S. PATENT DOCUMENTS

(73) Assignee: **Microchip Technology Incorporated,**
Chandler, AZ (US)

4,760,434 A * 7/1988 Tsuzuki H01L 23/34
257/470
5,304,837 A * 4/1994 Hierold H01L 27/0248
257/341
5,821,599 A 10/1998 Rupp 257/467
2004/0090726 A1 * 5/2004 Ball H02H 9/001
361/93.9
2007/0176212 A1 * 8/2007 Zundel G01K 7/186
374/E7.023

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 665 days.

(Continued)

(21) Appl. No.: **17/692,381**

(22) Filed: **Mar. 11, 2022**

OTHER PUBLICATIONS

(65) **Prior Publication Data**

International Search Report and Written Opinion, Application No. PCT/US2022/035071, 13 pages, Oct. 14, 2022.

US 2023/0015578 A1 Jan. 19, 2023

Primary Examiner — Igwe U Anya

Related U.S. Application Data

(74) Attorney, Agent, or Firm — SLAYDEN GRUBERT BEARD PLLC

(60) Provisional application No. 63/217,352, filed on Jul. 1, 2021.

(57) **ABSTRACT**

(51) **Int. Cl.**

G01K 7/16 (2006.01)
G01K 7/01 (2006.01)
H10D 86/00 (2025.01)
H10D 86/80 (2025.01)

A temperature sensor integrated in a transistor array, e.g., metal-oxide-semiconductor field-effect transistor (MOS-FET) array, is provided. The integrated temperature sensor may include a doped well region formed in a substrate (e.g., SiC substrate), a resistor gate formed over the doped well region, first and second sensor terminals conductively coupled to the doped well region on opposite sides of the resistor gate. The integrated temperature sensor includes a gate driver to apply a voltage to the resistor gate that affects a resistance of the doped well region below the resistor gate, and temperature analysis circuitry to determine a resistance of a conductive path passing through the doped well region, and determine a temperature associated with the transistor array.

(52) **U.S. Cl.**

CPC **G01K 7/16** (2013.01); **G01K 7/01** (2013.01); **H10D 86/00** (2025.01); **H10D 86/80** (2025.01); **G01K 2217/00** (2013.01)

(58) **Field of Classification Search**

CPC G01K 7/16; G01K 7/01; G01K 2217/00; H01L 27/0248; H01L 29/1608; H01L 29/7803; H01L 29/7838; H10D 86/00; H10D 86/80; H10D 84/141

21 Claims, 13 Drawing Sheets

