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Reiter et al.

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(54) **SYSTEM AND METHODS FOR RAMP CONTROL**

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,504,741 A	3/1985	Armitage	327/135
2010/0208112 A1 *	8/2010	Lim	G11C 7/1051
			348/294
2014/0014815 A1	1/2014	Lee et al.	250/208.1
2018/0323793 A1	11/2018	Onde et al.	
2021/0067723 A1 *	3/2021	Kim	H04N 25/78
2021/0068823 A1 *	3/2021	Nicholas	A61B 17/0686

OTHER PUBLICATIONS

International Search Report and Written Opinion, Application No. PCT/US2023/010786, 12 pages, May 16, 2023.

* cited by examiner

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CPC **H03M 1/56** (2013.01)

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See application file for complete search history.

(57) **ABSTRACT**

A device including an input to receive a clock signal, a ramp start program register, a ramp start active register, a ramp stop program register, a ramp stop active register, a ramp slope program register, a ramp slope active register, an update controller, the update controller to update, based on a programmable condition, respectively, the ramp start active register contents, the ramp stop active register contents and the ramp slope active register contents, and a ramp controller to generate a ramp signal, the ramp signal to begin at the value reflective of the ramp start active register contents, the ramp signal to change value at each cycle of the clock signal based on the value reflective of the ramp slope active register contents, and the ramp signal to stop at the value reflective of the ramp stop active register contents.

23 Claims, 5 Drawing Sheets

