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(54) **CONVERTERS AND RELATED APPARATUSES AND METHODS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 70 days.

This patent is subject to a terminal disclaimer.

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(56) **References Cited**

U.S. PATENT DOCUMENTS

5,705,919 A 1/1998 Wilcox
7,990,120 B2 8/2011 Leonard et al.
(Continued)

FOREIGN PATENT DOCUMENTS

CN 106300576 A 1/2017
CN 106953520 A 7/2017
(Continued)

OTHER PUBLICATIONS

International Search Report for Internation Application No. PCT/US2020/027296, dated Jul. 28, 2020, 4 pages.
(Continued)

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(57) **ABSTRACT**

Apparatuses and methods related to a converter are disclosed. An apparatus includes a converter and a controller. The converter converts an input voltage potential to an output voltage potential. The input voltage potential and the output voltage potential include direct current (DC) voltage potentials. The controller generates pulse width modulation (PWM) signals responsive to a duty cycle control signal, controls the converter via the PWM signals in a buck mode when the duty cycle control signal is less than a predetermined maximum buck value, and controls the converter via the PWM signals in a cascaded buck-boost mode (CBB mode) when the duty cycle control signal is greater than the predetermined maximum buck value. A duty cycle of at least a portion of the PWM signals transitions linearly with the duty cycle control signal from the buck mode to the CBB mode.

20 Claims, 28 Drawing Sheets